REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendments and the following remarks.

By the foregoing amendment, claims 1 and 2 have been amended. Claims 25-28 have been previously canceled, and claims 5-10 and 15-24 have been previously withdrawn. No new matter has been added by this Amendment. Thus, claims 1-4, 11-14 and 29-30 are currently pending in the application and subject to examination.

In the Office Action mailed June 20, 2006, claims 1, 2, 29 and 30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,907,357 to Maki in view of U.S. Patent No. 6,356,101 to Erstad. Claims 3, 4, and 11-14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Maki in view of Erstad and further in view of U.S. Patent No. 5,768,203 to Fuji. It is noted that claims 1 and 2 have been amended. To the extent that the rejections remain applicable to the claims currently pending, the Applicants hereby traverse the rejections, as follows.

In the Applicants' invention as recited in amended claim 1, a CMOS sensor circuit includes a photodiode; a reset transistor resetting said photodiode to an initial voltage; a voltage control circuit generating a reset signal in response to a reset control signal, the reset signal controlling a gate potential of said reset transistor to a potential other than power source potentials, wherein said voltage control circuit comprises an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor having a gate supplied with a first reset control signal, an N-channel MOS transistor having a gate supplied with a second reset control signal, and a transistor provided between a drain of said first P-channel MOS transistor and a drain of

said N-channel MOS transistor to control a blooming of the CMOS sensor circuit; and a delay circuit producing said first reset control signal which is supplied to the gate of the first P-channel MOS transistor, by delaying said second reset control signal supplied to the gate of the N-channel MOS transistor.

Thus, the delay circuit recited in claim 1 delays the second reset control signal supplied to the gate of the N-channel MOS transistor of the voltage control circuit to produce the first reset control signal supplied to the gate of the first P-channel MOS transistor of the voltage control circuit. A transistor is provided between the drain of the first P-channel MOS transistor and the drain of the N-channel MOS transistor to control blooming of the CMOS sensor circuit. The voltage control circuit generates a reset signal in response to a reset control signal, which controls a gate potential of the reset transistor of the CMOS sensor circuit. Thus, in the CMOS sensor circuit, when the reset control signal changes from a low level to a high level, the first P-channel MOS transistor turns OFF and the N-channel MOS transistor turns ON. In addition, a potential near the threshold potential of the transistor provided between the drains of the first P-channel MOS transistor and the N-channel MOS transistor is applied to the gate of the reset transistor. The reset transistor turns ON, and an excessive amount of electric charge accumulated in the photodiode can escape to a terminal of a reset voltage source via the reset transistor to restrain the blooming. By the claimed delay circuit, which produces the first reset control signal by delaying the second reset control signal, a time for clamping the reset voltage can be shortened, thereby enabling the charge from the photodiode to escape to the terminal of the reset voltage source via the reset transistor earlier.

The outstanding Office Action admits that Maki fails to disclose or suggest a delay circuit producing a first signal by delaying a second signal.

Erstad was cited as disclosing a glitch removal circuit for removing glitches from an inverter circuit using a delay line. However, Erstad does not cure the deficiencies of Maki described above. The delay line 207 of Erstad (Fig. 2) is connected to only one of the input terminals A and B of the logic block 202. Neither Maki nor Erstad teaches a delay circuit for use in a voltage control circuit which generates a reset signal in response to a reset control signal, in order to control blooming of a CMOS sensor circuit, wherein the delay circuit produces a first reset control signal supplied to the gate of a P-channel MOS transistor, by delaying a second reset control signal supplied to the gate of an N-channel MOS transistor.

Accordingly, neither Maki nor Erstad, alone or combined, discloses or suggests each and every feature recited in independent claim 1, as amended.

Fuji was not cited for, nor does Fuji cure the deficiencies that exist in the above combination.

Accordingly, none of the applied art of record, nor any combination thereof, discloses or suggests at least the combination of a voltage control circuit generating a reset signal in response to a reset control signal, the reset signal controlling a gate potential of said reset transistor to a potential other than power source potentials, wherein said voltage control circuit comprises an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor having a gate supplied with a first reset control signal, an N-channel MOS transistor having a gate supplied with a second reset control signal, and a transistor provided between a

drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor to control a blooming of the CMOS sensor circuit; and a delay circuit producing said first reset control signal which is supplied to the gate of the first P-channel MOS transistor, by delaying said second reset control signal supplied to the gate of the N-channel MOS transistor, as recited in claim 1, as amended.

For at least this reason, the Applicants respectfully submit that claim 1, as amended, is allowable over the applied art of record. As claim 1 is allowable, the Applicants submit that claims 3, 11, 13 and 29, which depend from allowable claim 1, are likewise allowable for at least the reasons set forth above with respect to claim 1.

Similarly, in the Applicants' invention as recited in amended claim 2, a CMOS sensor circuit includes a photodiode; a reset transistor resetting said photodiode to an initial voltage; a voltage control circuit generating a reset signal in response to a reset control signal, the reset signal keeping a gate potential of said reset transistor from completely becoming off, wherein said voltage control circuit comprises an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor having a gate supplied with a first reset control signal, an N-channel MOS transistor having a gate supplied with a second reset control signal, and a transistor provided between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor to control a blooming of the CMOS sensor circuit; and a delay circuit producing said first reset control signal which is supplied to the gate of the first P-channel MOS transistor, by delaying said second reset control signal supplied to the gate of the N-channel MOS transistor.

Thus, the delay circuit recited in claim 2 delays the second reset control signal supplied to the gate of the N-channel MOS transistor of the voltage control circuit to produce the first reset control signal supplied to the gate of the first P-channel MOS transistor of the voltage control circuit. A transistor is provided between the drain of the first P-channel MOS transistor and the drain of the N-channel MOS transistor to control blooming of the CMOS sensor circuit. The voltage control circuit generates a reset signal in response to a reset control signal, which controls a gate potential of the reset transistor of the CMOS sensor circuit. Thus, in the CMOS sensor circuit, when the reset control signal changes from a low level to a high level, the first P-channel MOS transistor turns OFF and the N-channel MOS transistor turns ON. In addition, a potential near the threshold potential of the transistor provided between the drains of the first P-channel MOS transistor and the N-channel MOS transistor is applied to the gate of the reset transistor. The reset transistor turns ON, and an excessive amount of electric charge accumulated in the photodiode can escape to a terminal of a reset voltage source via the reset transistor to restrain the blooming. By the claimed delay circuit, which produces the first reset control signal by delaying the second reset control signal, a time for clamping the reset voltage can be shortened, thereby enabling the charge from the photodiode to escape to the terminal of the reset voltage source via the reset transistor earlier.

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cure the deficiencies of Maki described above. The delay line 207 of Erstad (Fig. 2) is connected to only one of the input terminals A and B of the logic block 202. Neither Maki nor Erstad teaches a delay circuit for use in a voltage control circuit which generates a reset signal in response to a reset control signal, in order to control blooming of a CMOS sensor circuit, wherein the delay circuit produces a first reset control signal supplied to the gate of a P-channel MOS transistor, by delaying a second reset control signal supplied to the gate of an N-channel MOS transistor.

Accordingly, neither Maki nor Erstad, alone or combined, discloses or suggests each and every feature recited in independent claim 2, as amended.

Fuji was not cited for, nor does Fuji cure the deficiencies that exist in the above combination.

Accordingly, none of the applied art of record, nor any combination thereof, discloses or suggests at least the combination of a voltage control circuit generating a reset signal in response to a reset control signal, the reset signal keeping a gate potential of said reset transistor from completely becoming off, wherein said voltage control circuit comprises an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor having a gate supplied with a first reset control signal, an N-channel MOS transistor having a gate supplied with a second reset control signal, and a transistor provided between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor to control a blooming of the CMOS sensor circuit; and a delay circuit producing said first reset control signal which is supplied to the gate of the first P-channel MOS transistor, by

delaying said second reset control signal supplied to the gate of the N-channel MOS transistor, as recited in claim 2, as amended.

For at least this reason, the Applicants respectfully submit that claim 2, as amended, is allowable over the applied art of record. As claim 2 is allowable, the Applicants submit that claims 4, 12, 14 and 30, which depend from allowable claim 2, are likewise allowable for at least the reasons set forth above with respect to claim 2.

Conclusion

For all of the above reasons, it is respectfully submitted that the claims now pending patentably distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone Applicant's undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicant hereby petitions for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with

this communication to Deposit Account No. 01-2300, referring to client-matter number 100353-00095.

Respectfully submitted,

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Enclosures: Petition for Extension of Time (two months)